## REMARKS/ARGUMENTS

The Applicants have carefully considered this Application in connection with the Examiner's Action and respectfully request reconsideration of this Application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-20 in the Application. The Applicants previously amended Claims 1, 8 and 15 and canceled Claims 6, 13 and 20. In this response, the Applicants have amended Claims 1, 8 and 15. Accordingly, Claims 1-5, 7-12, and 14-19 are currently pending in the Application.

Support for the current amendments may be found, among other places, on page 21, Rule 2 of Table 2, of the present Application.

## I. Rejection of Claims 1-5 and 7-14 under 35 U.S.C. § 102

The Examiner has rejected Claims 1-5, and 7-14 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,683,547 to DeGroot ("DeGroot"). The Applicants respectfully contend that they have overcome this rejection, because DeGroot fails to teach each and every element of Claims 1-5, 7-12 and 14 as presently amended.

Claim 1 as currently amended comprises a rule, associated with an out-of-order completion logic, of never grouping an instruction that depends on a result of an older instruction. This rule has the following exceptions: wherein the instruction is a younger instruction and is a store or push operation, and wherein the older instruction is not a MAC instruction; or wherein the younger instruction is a multiply accumulate operation and the older instruction updates the accumulate stage.

DeGroot is generally directed to a data processing system that includes a multiple floating point arithmetic unit which purportedly includes a new instruction for handling multiple multiply or divide instructions. (Abstract).

The Examiner has stated that, in DeGroot: "Multiply and accumulate instructions are grouped to execute simultaneously such that a result produced by the ADD and Multiply units each cycle. One rule is that a maximum of two instructions may be grouped to produce results each cycle. Another rule is that only ready instructions are grouped to execute together." (Examiner's Action, page 3).

However, DeGroot does not teach the elements of amended Claim 1. Assuming, arguendo, that DeGroot does disclose, either expressly or implicitly, rules associated with an out-of order completion logic as claimed in Claim 1, DeGroot does not disclose or suggest a rule as claimed in independent amended Claim 1. The "rules" of DeGroot, as described by the Examiner, may be generally associated with pipelining instructions, but are not the rules as claimed in independent amended Claim 1.

In some embodiments, employment of the rule as claimed in independent amended Claim 1 may be advantageous in that it may aid breaking the MAC into independent stages, whereby the stages can be allocated independently to the execution of the grouped instructions, which can increase the overall throughput of the MAC of Claim 1.

DeGroot, therefore, does not anticipate Claim 1 as currently amended. By similar reasoning, DeGroot fails to anticipate each and every limitation of Claim 8. Claims 4-5 and 7-14 depend upon independent Claims 1 and 8, respectively. Therefore, Claims 1-5 and 7-14 are novel over DeGroot and are therefore allowable.

Accordingly, the Applicants respectfully request that the Examiner withdraw the rejection of Claims 1-5 and 7-14 under 35 U.S.C. § 102(b).

## II. Rejection of Claims 15-19 under 35 U.S.C. § 103

The Examiner has rejected Claims 15-19 under 35 U.S.C. § 103(a) as being unpatentable over DeGroot in view of U.S. Patent No. 4,683,547 to Chamdani, et al. (Chamdani). The Applicants contend that they overcome the rejection, because DeGroot and Chamdani, either singularly or in combination, fail to teach or suggest each and every element of Claims 15-19.

Amended independent Claim 15 comprises a rule, associated with an out-of-order completion logic, of never grouping an instruction that depends on a result of an older instruction. This rule has the following exceptions: wherein the instruction is a younger instruction and is a store or push operation, and wherein the older instruction is not a MAC instruction; or wherein the younger instruction is a multiply accumulate operation and the older instruction updates the accumulate stage.

The Examiner has again cited DeGroot for the proposition that DeGroot: "Multiply and accumulate instructions are grouped to execute simultaneously such that a result produced by the ADD and Multiply units each cycle. One rule is that a maximum of two instructions may be grouped to produce results each cycle. Another rule is that only ready instructions are grouped to execute together." (Examiner's Action, page 3). The Applicants respectfully contend that DeGroot does not disclose Claim 15 as amended, as discussed, above, concerning analogous language of Claim 1.

Nor does Chamdani compensate for the deficiencies of DeGroot. Chamdani is directed to a distributed instruction queue in a superscalar microprocessor that purportedly supports multi-instruction issue, decoupled data flow scheduling, out-of-order execution, register renaming, multi-level speculative execution, and precise interrupts. (Abstract). Chamdani is generally cited by the Examiner for an element of an at least four-wide instruction bus for the desirable purpose of achieving parallel execution within a processor. (Examiner's Action, page 3).

However, Chandani does not disclose or suggest a rule of never grouping an instruction that depends on a result of an older instruction, with the following exceptions: wherein the instruction is a younger instruction and is a store or push operation, and wherein the older instruction is not a MAC instruction; or wherein the younger instruction is a multiply accumulate operation and the older instruction updates the accumulate stage.

Therefore, both DeGroot and Chamdani, either separately or in combination, fail to teach or suggest each and every element of Claims 15-19

Accordingly, the Applicants respectfully request that the Examiner withdraw the rejection of Claims 15-19 under 35 U.S.C. 103(a) and allow issuance thereof.

Appl. No. 10/007,298 Reply to Examiner's Action dated June 20, 2006

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims

currently pending in this application to be in condition for allowance and therefore earnestly solicit a

Notice of Allowance for Claims 1-5, 7-12, and 14-19.

The Applicants request the Examiner to telephone the undersigned attorney of record at

(972) 480-8800 if such would further or expedite the prosecution of the present application. The

Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account

08-2395.

Respectfully submitted,

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11